THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAMES A. KAHLE, ET AL.

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Appeal No. 96-2607
Application 08/001,865[1]

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ON BRIEF

_____

Before THOMAS, HAIRSTON and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of

[1]Application for patent filed January 8, 1993.

claims 1 through 10, all of the claims pending in the present application.

The invention relates to a method and system for enhanced instruction dispatch in a superscaler processor system utilizing independently accessed intermediate storage. On pages 13 and 14 of the specification, Appellants disclose that Figure 3 illustrates the utilization of intermediate storage buffers within the superscaler processor system of Figure 1, in accordance with their invention. The plurality of intermediate storage buffers 20 are connected to one independent bus 64. Each of a plurality of execution units 24a, 24b and 24c are coupled to each of the multiple independent buses 64. Thus, when data is generated by the execution of an instruction within an execution unit, the execution unit places that data on a bus corresponding to a designed intermediate storage buffer which has been specified as a destination for that data, where the data is temporarily stored. On page 15 of the specification, Appellants disclose that the advantage of this arrangement is the elimination of the need to store the data in a buffer and then

thereafter access that data from the buffer. The ability to retrieve data directly from the bus will significantly increase the operation speed of the processing system.

The independent claim 1 is reproduced as follows:

> 1. A method for enhanced instruction dispatch efficiency in a superscalar processor system capable of fetching an application specified ordered sequence of scalar instruc-tions and simultaneously dispatching a group of said scalar instructions to a plurality of execution units, said method comprising the steps of:
>
> providing a plurality of intermediate storage buffers within said superscalar processor system;
>
> coupling each of said plurality of intermediate storage buffers to a11 of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers;
>
> dispatching selected ones of said group of scalar instructions to selected ones of said plurality of execution units on an opportunistic basis; and
>
> transferring a result of execution of each of said dispatched scalar instructions from one of said plurality of execution units to a designated one of said plurality of intermediate storage buffers via an associated independent bus, wherein said results may be stored without contention for access among said plurality of execution units and wherein said result is available to each of said plurality of execution units.

The Examiner relies on the following references:

Lawrie	4,051,551	Sep. 27, 1977
Johnson	5,136,697	Aug. 04, 1992

Claims 1 through 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Johnson and Lawrie. Rather than reiter- rate the arguments of Appellants and the Examiner, reference is made to the briefs[2] and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 10 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or

[2]Appellants filed an appeal brief on September 29, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on January 16, 1996. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated February 15, 1996 that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellants argue on pages 7 and 8 of the brief that Johnson and Lawrie, together or individually, fail to teach or suggest coupling of each of a plurality of intermediate storage buffers to all of a plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers. The Examiner argues on page 7 of the answer that it is irrelevant whether the reference teaches this limitation because this limitation is not recited in Appellants' claims.

Appellants responded in the reply brief that the

limitation cannot be ignored because the limitation is positively recited in the claims. We note that Appellants' claim 1 recites "coupling each of said plurality of intermediate storage buffers to all of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers" and 6 recites "means for coupling each of said plurality of intermediate storage buffers to all of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers." Thus, all of Appellants' independent claims recite this
limitation and thereby the Examiner has the burden to establish
why one having ordinary skill in the art would have been led to the claimed limitation by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions.

The Examiner further argues on page 7 of the answer that Lawrie teaches coupling each of said plurality of intermediate storage buffers to all of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers. The Examiner reasons that Lawrie teaches this limitation because Lawrie shows in Figure 3 a storage device coupled to all of the plurality of arithmetic units via a bus.

Upon a careful review of Lawrie, we find that the reference fails to teach the Appellants' recited limitation of coupling
each of said plurality of intermediate storage buffers to all of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers. In column 1, Lawrie teaches that the object of his invention is to provide non-conflicting linear vector storage of a multidimensional matrix in
a parallel memory computer system. In column 2, lines 49-58, Lawrie teaches that the present invention is understood by

considering a multidimensional matrix 11 pierced by a linear vector 13 shown in Figure 1. Lawrie states that the invention provides a method and apparatus for accessing in parallel all matrix elements along the vector 13. In column 3, lines 1 through 14, Lawrie teaches that Figure 3 shows the storage apparatus of their invention. The storage apparatus generates two indexing tags, T(D) and N(m). Tag T(D) aligns a particular memory 17 with a particular processor 19 and tag N(m) addresses memory 17. In column 4, line 56, through column 5, line 35, Lawrie teaches that the storage apparatus provides linear vector storage for a three dimensional matrix. It is clear that the storage apparatus is not providing the function of bus buffering as claimed in Appellants' claims.

Therefore, we fail to find that the references teach or suggest coupling each of said plurality of intermediate storage buffers to all of said plurality of execution units via an independent bus wherein each independent bus is associated with a single one of said plurality of intermediate storage buffers as recited in Appellants' claims. We are not inclined to dispense with proof by evidence when the

proposition at issue is not supported by a teaching in a prior art reference or common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966).

We have not sustained the rejection of claims 1 through 10 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
KENNETH W. HAIRSTON	)	APPEALS AND

Administrative Patent Judge	)	INTERFERENCES
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MICHAEL R. FLEMING	)	
Administrative Patent Judge	)	

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Application 08/001,865

Andrew J. Dillon
Felsman, Bradley, Gunter & Dillon
2600 Continental Plaza
777 Main Street
Fort Worth, TX 76102